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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,155	07/30/2003	Yi Ding	M-15222 US	1880
7.	590 04/01/2005	EXAMINER		
Michael Shenker			NHU, DAVID	
1.100	KWOK CHEN & HE	ART UNIT	PAPER NUMBER	
Suite 226 1762 Technology Drive San Jose, CA 95110			2818	
			DATE MAILED: 04/01/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

EX

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ② MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the precisions of 3 CPR 1.13(s), in no event, however, may a reply be timaly filled Extensions of time may be available under the precisions of 3 CPR 1.13(s), in no event, however, may a reply be timaly filled If the period for reply specified above is less than thirty (30) days, a reply within the statistory minimum of thinty (30) days will be considered timely. If the period for reply specified above is the statistic period will active property and ville gains (50) MONTHS from the mailtage date of this communication or property of the control of the communication of the communication or property of the communication of		Application No.	Applicant(s)				
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DETAILED ACTIONS

Election/Restrictions

1. Applicant's election of Group I (Claims 22-42) is acknowledge.

Claims 22-42 are remained for examination. Claims 1-21 are withdrawn from consideration as being directed to non-election invention. See 37 CFR 1.142 (b) and MPEP & 821.03.

Drawings

2. There is no bitline region 174 in figures 21A, 21B. There is also no description of layer 230 in figurers 16-17.

Claims Objection

3. Claim 22, "the substrate" should be -the semiconductor substrate--

Claims 29, 30, "the memory cell" should be -the nonvolatile memory cell--

Claim 29, "the channel portion" should be -the channel region--

Claim 33, "An method" should be - A method--

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 5. Claims 22-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Ogura et al (6,388,293 B1), and Harari et al (6,420,231 B1).

Regarding claim 22, Ogura, (see figures 1, 35, 14, col. 5, lines 50-67, col. 6, lines 1-67, col. 7, lines 1-53, col. 17, lines 28-67, col. 18, lines 1-21), teaches a method for

Art Unit: 2818

manufacturing an integrated circuit comprising a nonvolatile memory cell having source/drain regions 121, 122 of a first conductivity n-type in a semiconductor substrate 10 and having a channel region 110 in the semiconductor substrate between the source/drain regions, the method comprising: forming a first conductive gate 140 comprising a semiconductor material (polysilicon) of a second conductivity p-type opposite to the first conductivity n-type, the first conductive gate overlying a portion of the channel region 110; and forming a floating gate 140 overlying a portion of the channel region.

Regarding claims 23-32, Ogura, (see figures 1-5, col. 6-9, lines 1-67), also teaches the channel region comprises a surface region underlying the first conductive gate and having a lower dopant concentration of the second conductivity type than a region immediately below the surface region; the surface region is at 0.20 micro meter deep (see col.7, lines 37-43); implanting an impurity of the first conductivity type into a surface region of the channel region, wherein the surface region is to be below the first conductive gate; wherein the first conductive gate is to turn on the underlying portion of the channel region to provide access to the memory cell; wherein the floating gate is one of two floating gates of the nonvolatile memory cell, each floating gate overlying a portion of the channel region; wherein the first conductivity type is type N; wherein the second conductivity type is type P.

Regarding claim 22, Harari, (see figures 4, 5, col. 8, lines 1-39), teaches a method for manufacturing an integrated circuit comprising a nonvolatile memory cell having source/drain regions 49, 51 of a first conductivity type in a semiconductor substrate 45

Application/Control Number: 10/632,155

Art Unit: 2818

and having a channel region L1-L2 in the semiconductor substrate between the source/drain regions, the method comprising: forming a first conductive gate 55-58 comprising a semiconductor material of a second conductivity type opposite to the first conductivity type, the first conductive gate overlying a portion of the channel region; and forming a floating gate 55-58 overlying a portion of the channel region.

Regarding claim 23, Harari, (see col. 8, lines 15-18), teaches wherein the first conductive gate is a gate of a buried channel transistor.

Regarding claim 33, Ogura, (see figure 14, col. 17, lines 28-67), teaches a method for manufacturing an integrated circuit comprising a nonvolatile memory cell having source/drain region having source/drain regions 121, 122 of a first conductivity n-type in a semiconductor substrate 10 and having a channel region 110 in the semiconductor substrate between the source/drain regions, the method comprising: forming a first conductive gate 140 overlying a portion of the channel region 110; and forming a floating gate 140 overlying a portion of the channel region wherein the first conductive gate is a gate of a buried channel transistor.

Regarding claim 22, Harari, (see figures 4, 5, col. 8, lines 1-39), teaches a method for manufacturing an integrated circuit comprising a nonvolatile memory cell having source/drain regions 49, 51 of a first conductivity type in a semiconductor substrate 45 and having a channel region L1-L2 in the semiconductor substrate between the source/drain regions, the method comprising: forming a first conductive gate 55-58 comprising a semiconductor material of a second conductivity type opposite to the first conductivity type, the first conductive gate overlying a portion of the channel region; and

forming a floating gate 55-58 overlying a portion of the channel region, wherein the first conductive gate is a gate of a buried channel transistor.

Page 5

Regarding claims 34-42, Ogura, (see figures 1-5, col. 6-9, lines 1-67), also teaches the channel region comprises a surface region underlying the first conductive gate and having a lower dopant concentration of the second conductivity type than a region immediately below the surface region; the surface region is at 0.20 micro meter deep (see col.7, lines 37-43); implanting an impurity of the first conductivity type into a surface region of the channel region, wherein the surface region is to be below the first conductive gate; wherein the first conductive gate is to turn on the underlying portion of the channel region to provide access to the memory cell; wherein the floating gate is one of two floating gates of the nonvolatile memory cell, each floating gate overlying a portion of the channel region; wherein the first conductivity type is type N; wherein the second conductivity type is type P.

Conclusion

- 6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Eitan'725, Morii'979, Chang'115, Perlegos'776 are cited as of interest.
- 7. A shortened statutory period for response to this action is set to expired 3 (three) months from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see 710.02 (b)).
- 8. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu, (571)272-1792. The examiner can normally be reached on

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Art Unit: 2818

Monday-Friday from 7:30 AM to 5:00 PM. The examiner's supervisor, David Nelms can be reached on (571)272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703)872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the patent application information retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Nhu

March 24, 2005